REMARKS

In response to the Final Office Action mailed August 20, 2008, Applicants respectfully request reconsideration. All of the issues raised in the Office Action have been carefully considered and are addressed herein.

Claims 1-7 are pending in this application, of which claims 1 and 5 are independent claims. In this paper, no claims have been amended, added or canceled. The application as now presented is believed to be in allowable condition.

I. Rejections Under 35 U.S.C. §103

The Final Office Action rejects claims 1-7 under 35 U.S.C. §103(a) as purportedly being obvious over U.S. Patent No. 6,961,875 ("Floyd") in view of U.S. Patent No. 6,070,210 ("Cheon"). Applicants respectfully traverse each of these rejections.

A. Overview of Embodiments of the Present Invention

Embodiments of the present invention are directed to the monitoring and analysis of a microprocessor (page 1, lines 1-3). To check the proper operation of the microprocessor, a monitoring circuit integrated with the microprocessor transmits first digital messages to an analysis tool, wherein the first digital messages represent specific events that depend on the execution of instructions in the microprocessor (page 3, lines 15-17). As would be readily appreciated by one of ordinary skill in the art, a microprocessor instruction is multiple-bit data word (e.g., 8 bits, 16 bits, 32 bits, etc.) representing an action a microprocessor is to take (or in some cases not take), and/or containing data or information that the microprocessor is to act on, use, or manipulate pursuant to some previous instruction.

The monitoring circuit also transmits second digital messages to the analysis tool, wherein the second digital messages represent events that are independent of the operation of the microprocessor (page 6, lines 5-10). The second digital messages are only sent from the monitoring circuit to the analysis tool when the monitoring circuit is not sending first digital messages (i.e., when resource management conditions are fulfilled). That is, priority is given to sending first digital messages which relate to the microprocessor operation (page 7, lines 7-10).

The analysis tool distinguishes between the first digital messages and the second digital messages by examining an identifier included as part of the digital messages (page 6, lines 6-8).

It should be appreciated that the foregoing discussion of embodiments of the invention is provided merely to assist the Examiner in appreciating various aspects of the present invention. However, not all of the description provided above necessarily applies to each of the independent claims pending in the application. Therefore, the Examiner is requested not to rely upon the foregoing summary in interpreting any of the claims or in determining whether they patentably distinguish over the prior art of record, but rather is requested to rely only on the language of the claims themselves and the arguments specifically related thereto provided below.

B. Discussion of Floyd

Floyd is directed to a system for selectively recording multiple input logic signals as a function of time. Each logic signal consists of a sequence of single bits, wherein each bit represents a logic 0 or a logic 1. Floyd records the logic signals in a trace array integrated onto a VLSI chip to determine states of the logic signals at time points immediately proceeding a failure of the chip (Col. 2, lines 27-30; abstract). Due to the limited size of the trace array, the logic signals are only recorded when an event sequence signal is generated (Col. 2, lines 37-40). Event sequence signals are generated by an event logic based on a sequence of event signals generated by a logic circuit (Fig. 2). The logic circuit generates the event signals based on signals representing operation states in the VLSI chip (Col. 4, lines 24-27).

In one example, repeated writes to a particular location in memory on Floyd's VLSI chip may ultimately generate an error signal, and prior to the generation of the error signal, one or more sequences of input logic states are recoded in the trace array (Col. 4, lines 29-42). A counter counts a clock signal to create addresses for the trace array in which to store the states of the input logic signals (Col. 4, lines 43-58). Thus, the counter merely determines where the states of the input logic signals are stored in the trace array (Col. 4, lines 63-64). When an error in the VLSI chip occurs, the current counter value is stored in latches connected to the counter as an event address. The event address is the location in the trace array where the states of the input signals associated with the error signal are stored (Col. 4, line 65 – Col. 5, line 9). Thus, in the system of Floyd, logic signals, which represent a binary value (0 or 1) for specific control or

data signals in the logic unit of VLSI chip, are periodically recorded in the trace array in order to determine a sequence of events leading up to a chip failure.

C. The Office Action Fails to Establish a *Prima Facie* Case of Obviousness

MPEP §2143 lists several examples of rationales that may be used to establish a *prima facie* case of obviousness. The Office Action appears to rely on the first rationale, "(A) combining prior art elements according to known methods to yield predictable results," in support of the assertion that independent claims 1 and 5 are purportedly rendered obvious by Floyd and Cheon.

Section A of MPEP §2143 describes in detail the requirement for rejecting a claim based on this rationale. This section of the MPEP states that the Office Action **must** articulate the following: (1) a finding that the prior art included each element claimed, although not necessarily in a single prior art reference, with the only difference between the claimed invention and the prior art being the lack of actual combination of the elements in a single prior art reference, and (2) a finding that one of ordinary skill in the art could have combined the elements claimed by known methods, and that in combination, each element merely performs the same function as it does separately. The Office Action has failed to establish a *prima facie* case of obviousness, as the cited prior art fails to include each element claimed in each of the independent claims.

Claim 1 recites a method comprising transmitting first digital messages to an analysis tool from a monitoring circuit integrated with a microprocessor. The first digital messages are representative of first specific events which depend on execution of an instruction sequence by the microprocessor. The method further comprises detecting, with a request circuit, at least one second specific event independent from the execution of the instruction sequence by the microprocessor, and transmitting to the monitoring circuit, when the at least one second specific event is detected, a characteristic data signal associated with said at least one second specific event. The method further comprises storing the characteristic data signal in the monitoring circuit, and, if resource management conditions are fulfilled, transmitting an acknowledgement signal to the request circuit. The method further comprises transmitting at least one second digital message representative of the stored characteristic data signal to the analysis tool, and processing the first digital messages and the at least one second digital message via the analysis

tool to analyze operation of the microprocessor, including determining the instruction sequence executed by the microprocessor, and the at least one second specific event.

Claim 5 is an independent apparatus claim that closely tracks the language of independent method claim 1. Claim 5 recites an apparatus comprising a microprocessor, a memory integrated with the microprocessor, an analysis tool, and a monitoring circuit for transmitting first digital messages to the analysis tool. The first digital messages are representative of first specific events which depend on execution of an instruction sequence by the microprocessor. The apparatus further comprises a request circuit for detecting at least one second specific event independent from the execution of the instruction sequence by the microprocessor. The request circuit transmits to the monitoring circuit, when the at least one second specific event is detected, a request signal and a characteristic data signal associated with said at least one second specific event. The monitoring circuit stores the characteristic data signal, transmits to the request circuit an acknowledgement signal when the characteristic data signal is stored, and transmits to the analysis tool at least one second digital message representative of said stored characteristic data signal. The analysis tool processes the first digital messages and the at least one second digital message to analyze operation of the microprocessor, including determining the instruction sequence executed by the microprocessor, and the at least one second specific event.

The Office Action asserts that Floyd discloses at Fig. 2 and col. 4, lines 20-25 transmitting first digital messages to an analysis tool (trace array 207) from a monitoring circuit (counter 202) representative of first specific events (such as the event sequence signal 217) which depend on execution of an instruction sequence by a microprocessor (Office Action, page 2). Applicants respectfully disagree that the information transferred from counter 202 in Floyd to the trace array 207 represents first digital messages representative of first specific events which depend on execution of an instruction sequence by a microprocessor.

As shown in Fig. 2 of Floyd, K logic signals are stored in rows of trace array 207 when an event sequence signal is received at counter 201. The logic signals represent selective binary values in the logic unit of VLSI chip (Floyd, col. 1, lines 49-55). By comparing the actual sequence of recorded logic signals in the trace array with an expected sequence of logic signals,

events preceding the occurrence of an error (e.g., a failure) on the VLSI chip may be examined to determine why the error occurred (Floyd, col. 2, lines 59-61).

The only information that is transferred from the counter 202 to the trace array 207 of Floyd are addresses generated via an address decoder (Floyd, col. 4, lines 43-44). However, these addresses are not first digital messages representative of first specific events which depend on execution of an instruction sequence by a microprocessor, as recited in each of claims 1 and 5. Rather, the addresses merely indicate the location in which the input logic signals are to be stored in the trace array, and ***have no connection whatsoever to an instruction sequence of a microprocessor***. Accordingly, the trace array cannot use the addresses to infer anything about an instruction sequence of a microprocessor. In contrast, the first digital messages recited in claims 1 and 5 may be used by the analysis tool to analyze operation of the microprocessor, including determining the instruction sequence executed by the microprocessor.

The Office Action also asserts that Floyd discloses "first digital messages" and "second digital messages" as addresses 204 in Fig. 2, and "processing the first digital messages and the at least one second digital message via the analysis tool to analyze operation of the microprocessor, **including determining the instruction sequence executed by the microprocessor** (emphasis added)" as an instruction trace (Office Action, pages 2-3). Applicants respectfully disagree that the addresses 204 or the input logic signals 205 in Floyd are used to analyze operation of a microprocessor, including determining an instruction sequence executed by the microprocessor.

As discussed above, the addresses 204 of Floyd only indicate the location in which the input logic signals 205 are to be stored in the trace array, and have no connection whatsoever to an instruction sequence of a microprocessor. Furthermore, the Office Action appears to assert that the input logic signals 205 of Floyd form an instruction trace (Office Action, page 3). Applicants respectfully disagree that an ***instruction sequence*** executed by a microprocessor may be determined based upon the input logic signals of Floyd. Rather, the input logic signals in Floyd characterize the binary state of selected control and/or data signal values in the logic unit of a VLSI chip at a particular point in time (Floyd, col. 1, lines 49-55). The individual values of each of the input logical signals is considered when determining why an error signal in the VLSI chip was generated, but collectively, the sequence or trace of input logic signals has no higher level cohesive meaning, such that analysis of a trace could be used to determine an instruction

sequence executed by the microprocessor. In contrast, the first digital messages in embodiments of the present invention, and recited in claims 1 and 5, contain information that allows the analysis tool to determine an instruction sequence executed by the microprocessor.

Cheon fails to cure these deficiencies of Floyd. As discussed in a previous response to an Office Action dated February 6, 2008, Cheon fails to disclose or suggest determining an instruction sequence executed by a microprocessor. In Cheon, a microprocessor sends a "low" state or "high" state mode selection control signal to buffers 210 and 220 in circuitry associated with the DMA device to enable or disable acknowledgement signals DACK and BACK transferred between the SCSI controller and the DMA device. The state of the mode selection control signal, and thus which acknowledgement signal is active, determines the timing mode (i.e., single vs. burst mode) used to transfer data from the DMA device to the memory (Cheon, Fig. 2 and accompanying text at col. 3, line 65 – col. 4 line 26). Clearly this single control signal sent by the microprocessor of Cheon to change the timing mode of data transfer cannot be used by the memory to determine an instruction sequence executed by the microprocessor, as recited in claims 1 and 5.

As neither Floyd nor Cheon discloses or suggests processing first digital messages and the at least one second digital message via the analysis tool to analyze operation of the microprocessor, including determining the instruction sequence executed by the microprocessor, the Office Action fails to satisfy the requirements for establishing a *prima facie* case of obviousness regarding claims 1 and 5. Accordingly, Applicants respectfully submit that the rejection of each of claims 1 and 5 is improper, and should be withdrawn.

Claims 2-4 depend from claim 1 and claims 6 and 7 depend from claim 5. Each of these dependent claims patentably distinguishes over Floyd and Cheon for at least the same reasons as its respective base claim. Accordingly, it is respectfully requested that the rejection of each of these dependent claims be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, the Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 23/2825, under Docket No. S1022.81243US00.

Dated: October 27, 2008

Respectfully submitted,

By: _____

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